

INTRODUCTION

This application note applies to the following products:

T1 FRAMERS	T1 SCTs
DS2141A	DS2151
DS21Q41B	DS2152
DS21Q42	DS21352
DS21FF42	DS21552
DS21FT42	DS21Q352
	DS21Q552

In a SLC-96-based transmission scheme, the standard Fs-bit pattern is robbed to make room for a set of message fields. The SLC-96 multiframe is made up of six D4 superframes, so it is 72 frames long. In the 72-frame SLC-96 multiframe, 36 of the framing bits are the normal Ft pattern and the other 36 bits are divided into alarm, maintenance, spoiler, and concentrator bits, as well as 12 bits of the normal Fs pattern. Please see the Bellcore document TR-TSY-000008 for more details about SLC-96.

RECEIVE-SIDE SLC-96 APPLICATIONS

To enable the device to synchronize onto a SLC-96 pattern, the following configuration should be used:

- Set to D4 framing mode CCR2.3 = 0
- Set to cross-couple Ft and Fs bits RCR1.3 = 1
- Set to minimum sync time RCR1.2 = 0

The user has the option to either extract the SLC-96 message fields from the on-board RFDL register or via the external RLINK pin. The information is always available at both locations. If the user wishes to extract the message bits via the RLINK pin, then some hardware must be added to decode the bits. The SLC-96 message bits can be extracted via the RFDL register without any additional hardware and it is this method that this application note addresses.

Figure 1 describes the method used to extract the SLC-96 message bits. The devices contain an on-board SLC-96 synchronizer that is enabled when the CCR2.1 bit is set to one. In this mode, the match flag (SR2.2) takes on a new meaning; it will indicate when the framer has received the 12-bit Fs pattern that exists in SLC-96 multiframe. In each SLC-96 multiframe, the user will read the RFDL register three times. The external controller will wait for the match flag to be set. Once set, the controller will then wait for the RFDL to fill.

Figure 2 details how the SLC-96 fields will be represented in the RFDL register on each read. Since the RFDL is also used in the ESF framing mode, the zero destuffer should be disabled (CCR2.0 = 0). (**Note:** The match registers (RFDLM1 and RFDLM2) are not used in SLC-96 mode and can be programmed with any value.)

Figure 1. SLC-96 Message Field Extraction via RFDL

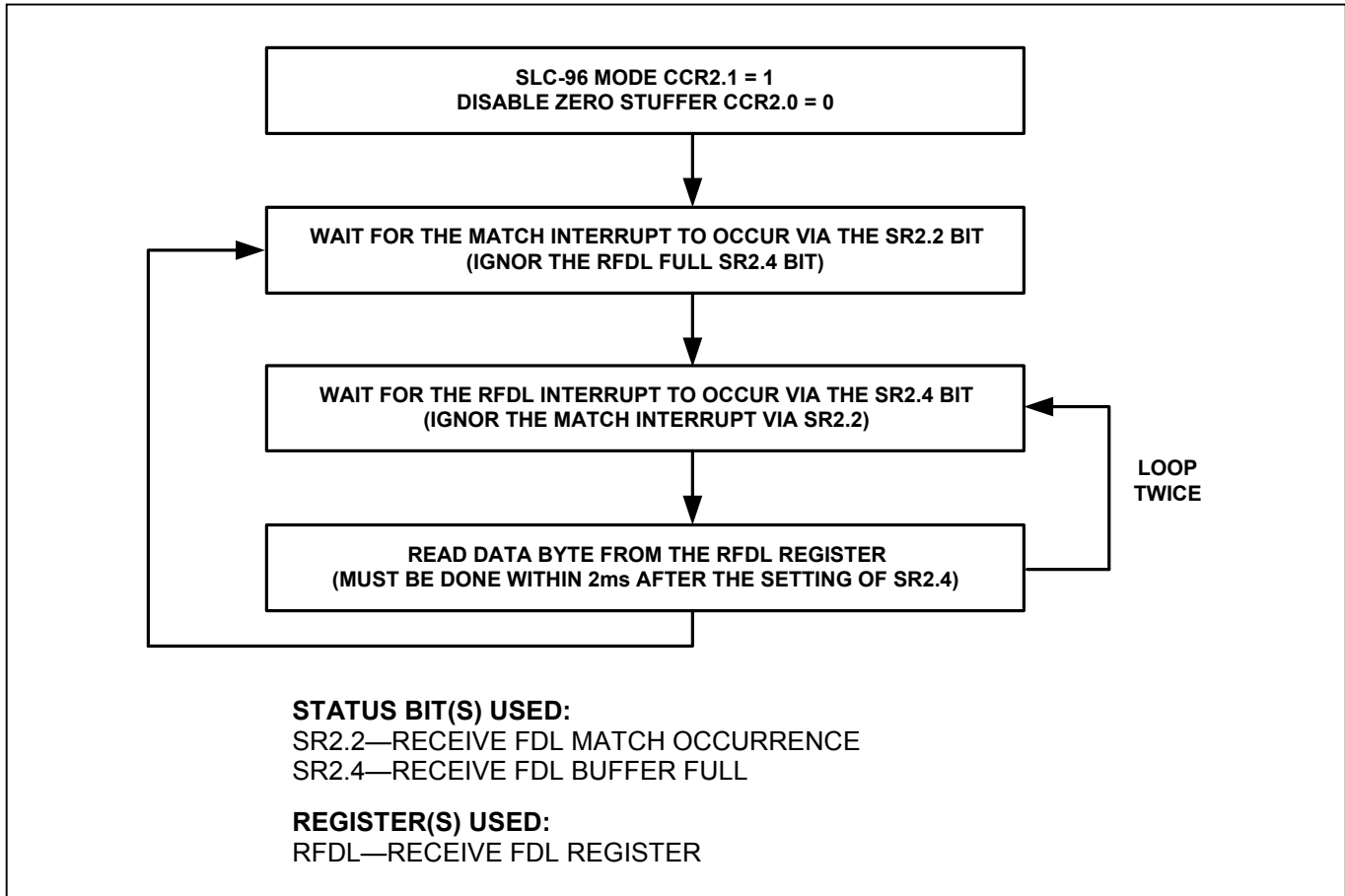


Figure 2. RFDL Register Byte Sequence

	(MSB)							(LSB)
READ #1	C8	C7	C6	C5	C4	C3	C2	C1
READ #2	M2	M1	S = 0	S = 1	S = 0	C11	C10	C9
READ #3	S = 1	S4	S3	S2	S1	A2	A1	M3

TRANSMIT-SIDE SLC-96 APPLICATIONS

To insert the SLC-96 message fields, the user has the option to either use the external TLINK pin or to use the onboard TFDL register. Usage of the TLINK pin will require some external hardware and to enable this option, the TCR1.2 bit should be set to one. This application note concerns itself solely to the use of the TFDL register to insert the SLC-96 message fields.

Figure 3 displays the method to enable the device to insert the SLC-96 message fields via the TFDL register. On each normal D4 multiframe boundary, the framer will signal to the user via the SR2.6 bit to write to the TFDL the sequence of bytes shown in Figure 4. The user will write to the TFDL six times in each SLC-96 multiframe.

Figure 3. SLC-96 Message Field Insertion via TFDL

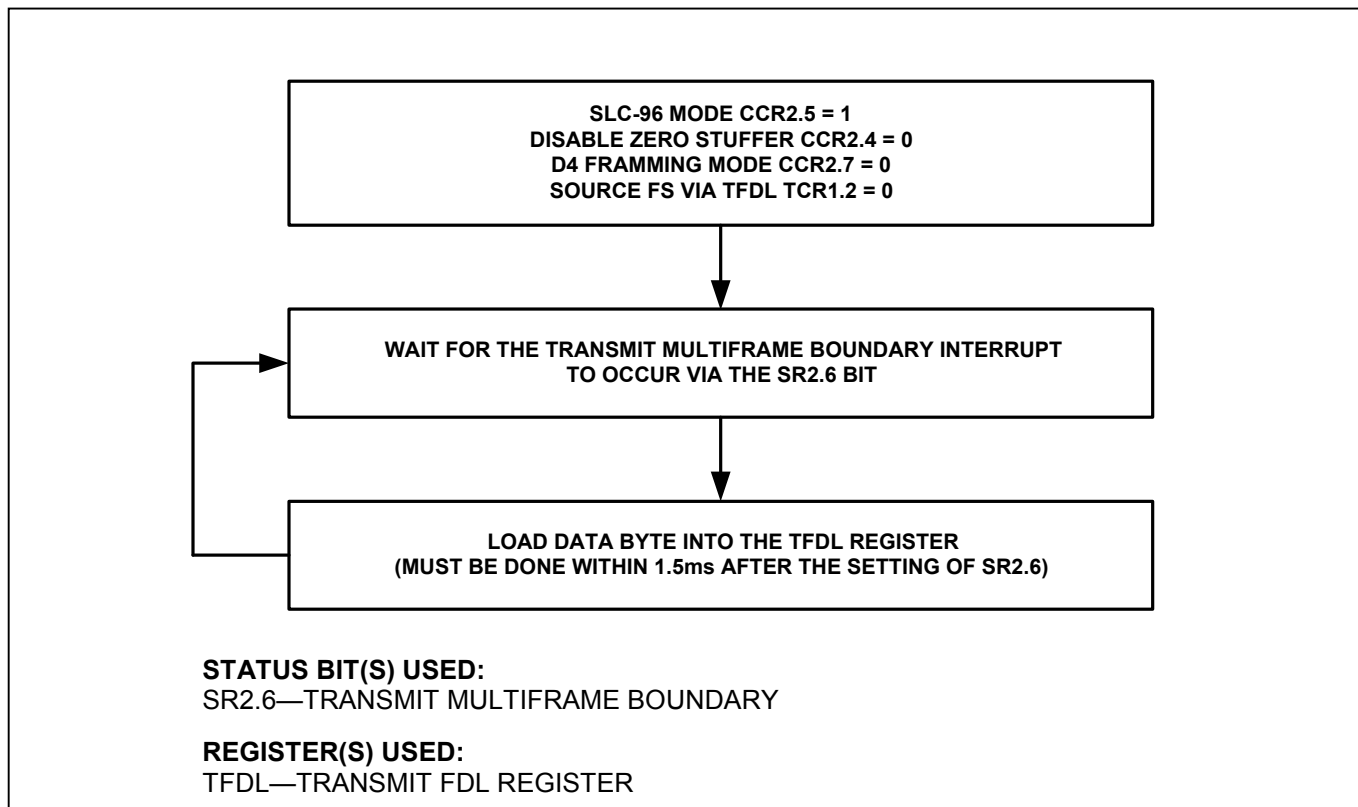


Figure 4. TFDL Register Byte Sequence

	(MSB)							(LSB)
Write #1	X	X	C1	1	1	1	0	0
Write #2	X	X	C7	C6	C5	C4	C3	C2
Write #3	X	X	S = 1	S = 0	C11	C10	C9	C8
Write #4	X	X	A2	A1	M3	M2	M1	S = 0
Write #5	X	X	0	S = 1	S4	S3	S2	S1
Write #6	X	X	0	1	1	1	0	0

T1 FRAMER AND SINGLE-CHIP TRANSCEIVER INFORMATION

For more information about Dallas Semiconductor's T1/E1 framers and single-chip transceivers, please consult the data sheets available on our website at www.maxim-ic.com/telecom.

If you have further questions concerning the operation of Dallas Semiconductor's T1/E1 framers and single-chip transceivers, please contact the Telecommunication Applications support team via email telecom.support@dalsemi.com or call 972-371-6555.